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Simulation of nonequilibrium thermal effects in power LDMOS transistors

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Abstract

The present work considers electrothermal simulation of LDMOS devices and associated nonequilibrium effects. Simulations have been performed on three kinds of LDMOS: bulk Si, partial SOI and full SOI. Differences between equilibrium and nonequilibrium modeling approaches are examined. The extent and significance of thermal nonequilibrium is determined from phonon temperature distributions obtained using a common electronic solution and three different heating models (Joule heating, electron/lattice scattering, phonon scattering). The results indicate that, under similar operating conditions, nonequilibrium behavior is more significant in the case of full SOI devices, where the extent of nonequilibrium is estimated to be twice that of the partial SOI device and four times that of the bulk device. Time development of acoustic phonon and lattice temperatures in the electrically active region indicates that nonequilibrium effects are significant for times less than 10 ns.

1. Introduction

Metal oxide semiconductor field effect transistors (MOSFETs) are widely used in a variety of power electronic systems. For example, the devices are particularly useful as high speed switches because of their low on-state resistance [1]. In high-frequency RF applications, they exhibit low capacitance and high gain (in lateral double-diffused MOS) or high stability (in vertical double-diffused MOS) [2]. MOSFETs can also be integrated with signal processing circuits to form "smart chips" and in-system programmable large-scale integration devices (IPLSI) [3]. The present work focuses on lateral double-diffused MOS (LDMOS), which is well suited for high frequency applications such as telecommunication circuits. These lateral surface effect devices are, however, susceptible to hot-carrier currents that induce several breakdown mechanisms. Various efforts have been directed towards characterizing hot-carrier effects in LDMOS, and suggestions have been made to mitigate such effects [4–6]. These attempts represent modest improvements in thermal management, but the devices are still likely to exhibit thermal problems. Therefore, thermal simulations of LDMOS are crucial for accurate estimates of device performance.

Nonequilibrium in power devices can be defined from an electrical and a thermal perspective. Electrical nonequilibrium includes all conditions that eventually cause a flow of charge (i.e. a current) [7]. However, the energy gained by charge carriers due to an externally applied electrical field, can be transferred to the lattice. In equilibrium, the electrons and lattice exhibit similar energy levels. Yet, power device operation requires the application of large fields and high currents. Therefore, these devices normally operate in electrical nonequilibrium.

Thermal nonequilibrium refers to the condition when charge carriers are not able to transfer their excess energy to the lattice efficiently. A temperature difference is created between electrons and the lattice resulting in localized heating in the active area of the device. At small scales, thermal transport in semiconductors is usually described in terms of quantized lattice vibrations

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Nomenclature

C	bulk thermal capacitance of Si (J/kg K)	T_A	acoustic phonon temperature (K)
C_A	acoustic phonon thermal capacitance (J/kg K)	T_{LO}	longitudinal optical phonon temperature (K)
C_{LO}	longitudinal optical phonon thermal capacitance (J/kg K)	T_L	lattice temperature (K)
D	thermal diffusivity (cm^2/s)	S	energy flux (J/cm^2)
H	generation term in bulk conduction equation (W/cm^3)	V	voltage (V)
J	current density (A/cm^2)	v	carrier velocity (cm/s)
k	bulk thermal conductivity of Si (W/cm K)	W	energy density loss rate (W/cm^2 s)
k_A	thermal conductivity of acoustic phonons (W/cm K)	ε	local permittivity (F/cm)
k_b	Boltzmann constant (1.38×10^{-23} J/K)	μ	mobility (cm^2/V s)
m^*	effective mass (kg)	η	carrier density (cm^{-3})
N_D	doping concentration (cm^{-3})	κ	electron thermal conductivity (W/cm K)
q	electron charge (1.6×10^{-19} C)	Ψ	electrostatic potential (V)
		ρ	local space charge density (cm^{-3})
		τ_{e-L}	electron–lattice scattering time constant (s)

called phonons. Energy transfer from electrons to the high-energy optical phonons is very efficient. However, optical phonons possess negligible group velocity and thus do not participate significantly in heat diffusion. They instead must transfer their energy to acoustic phonons, which diffuse heat. The energy transfer between phonons is relatively slow compared to electron-optical phonon transport, and thus, thermal nonequilibrium may also exist between optical and acoustic phonons. Fig. 1 shows the primary path of thermal energy transport and associated scattering time constants.

Numerical simulations are widely used to understand device operation and to predict nonequilibrium behavior in submicron devices because the length and time scales involved are not easily amenable to experimental analysis. Thus, the simulation models should be as accurate and physical as possible. Apanovich et al. [8] report that

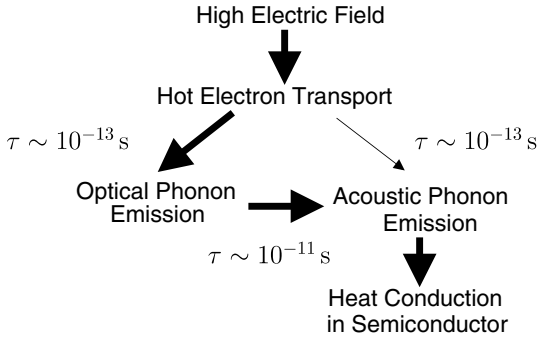

Fig. 1. The most likely path between energy carrying particles in a semiconductor device is shown with the corresponding scattering time constants.

the coupling between nonlocal charge transport and nonisothermal effects is significant in full SOI devices due to the low thermal conductivity of the buried oxide and the parasitic bipolar effect. Nonisothermal models were found to predict impact ionization and secondary breakdown more accurately than isothermal models, thus highlighting the influence of lattice heating on the electrical behavior of devices. Wachutka [9] describes the source of nonisothermal effects in electronic devices in great detail. Wachutka's model for thermal characterization of devices includes several nonequilibrium phenomena such as generation/recombination, Joule heating and Thomson heating. However, the model does not account for thermal nonequilibrium in which the energy of different vibrational modes is significantly different.

Lai and Majumdar [10] developed a coupled electrothermal model for studying thermal nonequilibrium in submicron silicon MOSFETs. Their results showed that the highest electron and lattice temperatures occur under the drain side of the gate electrode, which also corresponds to the region of highest electric field, and in turn the region where nonequilibrium effects such as impact ionization and velocity overshoot are maximum. Majumdar et al. [11] have analyzed the variation of hot electron and associated hot phonon effects in GaAs MESFETs. These hot carrier effects were observed to decrease the output drain current by as much as 15%. Thus, they conclude that both electron and lattice heating should be included in the analysis of electrical behavior of a device. Leung et al. [12] compared the different mechanisms of self-heating in full SOI LDMOS and determined that Joule heating is the dominant source of heat in these majority carrier devices. Re-

combination heating was found to be negligible in comparison.

An important structural modification that has been suggested to overcome some of the inherent deficiencies of bulk Si LDMOS and full SOI is the partial SOI device. Bulk Si LDMOS, though possessing excellent thermal conduction properties, often suffers from large leakage currents. Full SOI devices were developed to isolate electrical activity. The buried oxide layer in these devices acts as an electrical insulator that minimizes leakage currents. However, the oxide layer also acts as a barrier to thermal dissipation. This spatial confinement of thermal heating can adversely affect the electrical performance of the device. In contrast to full SOI, the buried oxide layer in partial SOI does not extend across the entire length of the device. Instead, a silicon window under the drain region provides a path for heat to diffuse away from the electrically active region.

The present work compares the behavior of three types of LDMOS, i.e. bulk Si, full SOI and partial SOI, to determine the extent of nonequilibrium in each case. The full SOI and partial SOI devices were analyzed with the intent of studying the influence of an insulator (oxide) layer within the device. DC simulations were performed to study the static behavior of the devices. Their thermal characteristics were compared to obtain qualitative information about nonequilibrium effects. The simulations were performed in a partially coupled manner. The electrical characteristics were analyzed using a commercial package (ATLAS [13]), while the thermal behavior was studied using a custom phonon solver. The drain current–drain voltage (I_d–V_d) and temperature comparison plots for the three devices and the conclusions drawn from them are presented.

Lim et al. [14] have earlier reported a comparison between self heating effects in thin SOI and partial SOI devices, under both steady-state and transient conditions. However, the present work investigates the validity of three different thermal models. The first assumes bulk diffusion and Joule heating as a source term. The second assumes bulk diffusion but uses a scattering term as the source term. The final model allows for thermal nonequilibrium using moments of the Boltzmann transport equations (BTE). This model incorporates multiple vibrational modes of the lattice and corresponding scattering between particles.

2. Device structure

The device structure and behavior was modeled after that of Perugupalli et al. [15] but incorporated certain modifications in doping profiles and structure of the gate oxide layer. Fig. 2 shows device structure with approximate doping wells along with the partial SOI layer. The length of this layer was treated as a free parameter in the present study. The threshold voltage was designed to be $V_t \approx 2.5$ V. The full SOI and partial SOI devices were based on the bulk device and had comparable threshold voltages. Device characteristics are listed in Table 1.

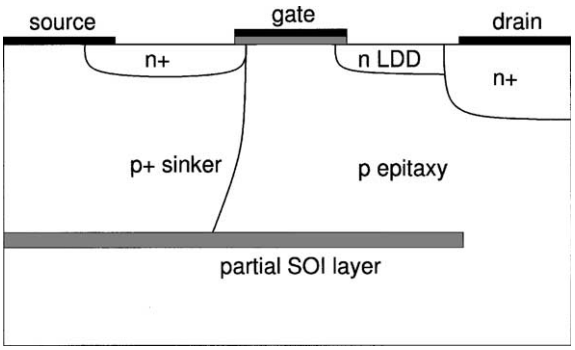

Fig. 2. Cross-sectional view of the partial SOI device with doping profile. The full SOI and bulk devices are the same except for the length of the SOI layer.

Gaussian doping profiles were used in these simulations with appropriate x- and y-direction roll-off distances. The source and drain regions were doped with $10^{20}/cm^3$ of phosphorus while the lightly doped drain (LDD) region (Fig. 2) was doped with $10^{17}/cm^3$ of phosphorus. The substrate region in each device was doped with $10^{15}/cm^3$ of boron. The p^+ sinker and p body were doped with $10^{19}/cm^3$ and $1.5 \times 10^{17}/cm^3$ boron respectively (Fig. 2). Note that the buried oxide layer was introduced into the structure of partial SOI and full SOI devices in order to study the effect of an insulator inside the device. Thus, all three devices were designed to have the same dimensions and doping profiles. The source and drain contacts of the devices were aluminum and were considered to be Ohmic contacts. For the sake of simplicity, the gate was also aluminum and the corresponding work function was adjusted to fix the threshold voltage. The computational mesh was refined, especially in regions of large gradients until numerical convergence was observed. Further, element sizes were kept below the Debye length of the active region to minimize discretization errors [10].

Table 1
Device dimensions

Parameter	Value (μm)
Source length	3.0
Source–gate spacing	3.25
Gate length	3.0
Gate–drain spacing	3.0
Drain length	3.0
Gate oxide thickness	0.065
Buried oxide depth	5.0

3. Simulation methodology

In this work, 2-D simulations were performed in a partially coupled manner to analyze the electrical and thermal characteristics of the devices. The commercial simulator (ATLAS) was used to perform the electrical characterization. Results from the electrical analysis, such as electron concentrations and electron temperatures, were imported into an in-house semiconductor heating model. Therefore, the results of the electronic solution were used as thermal source terms in the thermal solution. The results of the thermal solution are not coupled back to the electrical analysis. This uncoupled approach is similar to that of Sverdrup et al. [16] in that qualitative conclusions can be drawn from the results. Efforts are underway to couple the electrical and thermal solvers in order to obtain more accurate (and quantitative) results.

3.1. Electrical simulations

DC simulations were performed to obtain I_d–V_d characteristics of the devices. Electrical characteristics were found using the energy balance model in ATLAS [13] with the lattice heat diffusion equation. The gate voltages were chosen to be 4, 8 and 16 V in each case. At each gate voltage the drain voltage was stepped up from 1 to 20 V in increments of 1 V. Comparative electrical studies were performed on the devices under similar operating conditions (e.g., at a drain voltage of 20 V for each gate voltage). All electrical simulations were performed at steady-state.

The energy balance model used in this study is essentially the hydrodynamic model along with the lattice heating equation. It incorporates effects such as diffusion associated with carrier temperatures and dependence of impact ionization rates on carrier energy distributions [13]. This model consists of Poisson's equation for determining the electric field distribution and the carrier continuity equations for determining the carrier concentrations. These equations are solved in the silicon region only. The equations used for energy flux and current density are given as

$$\nabla \vec{S} = -\vec{J}\nabla\Psi - W - \frac{3k_b}{2}\frac{\partial}{\partial t}(nT_n) \tag{1}$$

$$\vec{J} = qD\nabla n - \mu n\nabla\Psi + qnD_n^T\nabla T_n \tag{2}$$

$$\vec{S} = -\kappa\nabla T_n - \frac{k_b}{q}\vec{J}T_n \tag{3}$$

Accurate MOSFET simulations call for the use of inversion-layer-specific mobility models. This requirement is due to the high scattering that occurs near the channel-gate oxide interface. In this simulation, a comprehensive model that takes into account the effect of transverse electric field, doping profile and carrier temperature distribution was employed. The model also includes the dependence of mobility on the parallel electric field, which is important near carrier saturation velocities.

The lattice heat diffusion equation given as

$$C\frac{\partial T_L}{\partial t} = \nabla\cdot(k\nabla T_L) + H \tag{4}$$

was included to determine the extent of energy transfer between the carrier and the lattice, and to study the variation of lattice temperatures (T_L) with input bias. Here H is the heat source and is modeled after the rigorous physical model proposed by Wachutka [9]. It includes carrier effects such as generation–recombination, impact ionization, Joule heating and Peltier and Thomson effects. A constant temperature sink (300 K) was used as the thermal boundary at the bottom of the device. All other boundaries were considered to be insulated. Nonlocal transport effects in the device were modeled by including Selberherr's model for impact ionization and the Shockley–Read–Hall model for carrier recombination.

The temperatures considered here are the local lattice temperatures. ATLAS has several built-in relations for determining properties based on local lattice temperatures. However, constant properties were used to simplify the analysis and to facilitate comparison. The temperature-dependent lifetime of the carriers in the recombination model was assumed to be the default value of 10^{-7} s.

3.2. Thermal simulations

Determination of nonequilibrium energies and momenta of particles requires a solution of the Boltzmann transport equations (BTE)

$$\frac{\partial f}{\partial t} + \vec{v}\cdot\nabla f + \vec{F}\cdot\frac{\partial f}{\partial \vec{p}} = \left(\frac{\partial f}{\partial t}\right)_{\text{scat}} \tag{5}$$

where f represents the distribution of particles, p represents the momentum vector and F is the force applied on the system by the electric field. The right side represents the rate of change of the particle distribution due to scattering. Solving the transport equation directly requires substantial computational effort; therefore researchers have simplified the system by taking moments of the BTE. The resulting equations are often called the hydrodynamic equations of electron and phonon transport [10]. The hydrodynamic equations are derived from the BTE by employing the relaxation time approximation and taking appropriate moments for momentum and energy of each particle including the different phonon modes. Under the relaxation time ap-

proximation, the scattering term of the BTE is given in terms of a momentum dependent scattering time constant

$$\left(\frac{\partial f}{\partial t}\right)_{\text{scat}} = \frac{f_{\text{eq}} - f}{\tau(\mathbf{r}, \mathbf{p})} \tag{6}$$

where f_{eq} represents the equilibrium distribution. As a device is driven further from equilibrium, the magnitude of the scattering term will increase.

In the present work, thermal analysis of the devices consisted of solving the energy equations for optical and acoustic phonons using a custom developed code. The primary path of energy transport is represented by first scattering between electrons and optical phonons (T_{LO}) and then optical phonons to the lattice (T_{A}) [17]:

$$C_{\text{LO}}\frac{\partial T_{\text{LO}}}{\partial t} = \frac{3\rho k_{\text{b}}}{2}\left(\frac{T_{\text{e}} - T_{\text{L}}}{\tau_{\text{e-L}}}\right) + \frac{\rho m^* v^2}{2\tau_{\text{e-LO}}} - C_{\text{LO}}\left(\frac{T_{\text{LO}} - T_{\text{A}}}{\tau_{\text{LO-A}}}\right) \tag{7}$$

$$C_{\text{A}}\frac{\partial T_{\text{A}}}{\partial t} = \nabla \cdot (k_{\text{A}} \nabla T_{\text{A}}) + C_{\text{LO}}\left(\frac{T_{\text{LO}} - T_{\text{A}}}{\tau_{\text{LO-A}}}\right) + \frac{3\rho k_{\text{b}}}{2}\left(\frac{T_{\text{e}} - T_{\text{L}}}{\tau_{\text{e-L}}}\right) \tag{8}$$

Here, C_{LO} and C_{A} represent the heat capacity of optical and acoustic phonons respectively. Note that acoustic phonons possess finite group velocity and participate in heat diffusion. Optical phonons, however, have negligible group velocity and cannot diffuse heat. They provide an efficient intermediate path for heat transfer from the source (electrons) to the sink (acoustic phonons). With this approach, the lattice temperature is often thought to be equivalent to the acoustic phonon temperature. The electron temperature (T_{e}) in Eqs. (7) and (8) is obtained from ATLAS, along with the carrier concentration ρ.

The time constants used in solving the energy equations greatly influence the degree of nonequilibrium [18] and the accuracy of the results. In the present work, the time constants are taken as $\tau_{\text{e-LO}} = 0.1$ ps [17] and $\tau_{\text{LO-A}} = 10$ ps [7].

The value of the time constant can have a significant impact on the solution. However, these constant values are reasonable and should not affect the qualitative arguments to be presented later.

Thermal analysis software was developed from a commercially available, object-oriented general PDE solution library (Diffpack) [19]. The analysis was performed for very short time steps (~1 ps to 1 ns) to study the transient behavior of phonons. The time development of the two phonons for long periods (toward steady-state) was also studied. We note that results of the electrical simulation were for steady-state conditions. Thus, transient electrical effects are ignored by assumption. Even though this approach cannot be rigorously justified, the resulting simulation technique does provide at least a qualitative understanding of equilibrium and nonequilibrium thermal transport in real devices.

The thermal boundary conditions applied are insulated on all sides of the device except the bottom, which is specified to be 300 K. The insulated conditions can be approximately justified if we assume that the device under consideration does not operate alone. If neighboring devices operate with the same thermal dissipation, a symmetry boundary can be used. On the top surface, the layers of oxide and packaging limit the diffusion of thermal energy, and the insulated condition is a convenient approximation of this condition.

To ensure that the energy calculations based on the different models do not bias the comparison, an energy balance is performed between the ATLAS and Diffpack simulations. This analysis determines if the overall thermal energy is the same, and that different thermal distributions are created only due to the difference in device phenomena. For all cases examined, the steady-state energy generation in the device and the heat flux leaving the bottom of the device were within 5% of each other. Although the formulation is not expected to conserve energy because of the lack of coupling, the agreement between models is remarkable. Therefore, it is assumed that the models are all self-consistent.

The focus of the nonequilibrium analysis was to determine the differences in the thermal source terms used in the different models. The three cases are described as Joule heating, electron–lattice scattering and the phonon model. Although each model can be shown to be equivalent under certain instances of equilibrium, under nonequilibrium conditions the results of the three models can vary significantly.

3.2.1. Case 1: Joule heating

The thermal model consists of the heat diffusion equation using a Joule heating term as the source (see Eq. (4)). The source term is computed from the electrical solution as the product of the local field and current density.

$$H = \vec{J} \cdot \vec{E} \tag{9}$$

This source term is similar to the one used by Leung et al. [12] and assumes that recombination heating is negligible. In this case, the "hot spot" will occur near the location where the dot product of the field and current density is largest. Previous simulations and intuition suggest that the bulk of the heating will occur directly under the gate region, where most of the voltage drop occurs and where the current density will be large because of the restricted electron flow path due to the depletion region. LDD devices are designed to decrease

the localized heating by lightly doping the region between the gate and the drain so that the voltage drop is spread over a larger area. Therefore, the location of heating for the present device is expected to occur on the drain side of the gate.

3.2.2. Case 2: electron–lattice scattering

In this case, the thermal system is represented as a single lattice temperature and is considered to be in thermal equilibrium. However, we have assumed that the heat generation is due to nonequilibrium electron temperatures. The source then is a scattering term obtained from the relaxation-time approximation and moments of the BTE. In essence, the transport is similar to case 1 in that the heat diffusion equation governs transport in the solid (Eq. (4)), except the source term is now given as a moment of the relaxation time approximation from Eq. (6).

$$H = \frac{3\rho k_b}{2}\left(\frac{T_e - T_L}{\tau_{e-L}}\right) \tag{10}$$

In the present work, the momentum dependence of the scattering rate is ignored and τ_{e-L} is treated as a true constant.

3.2.3. Case 3: phonon model

Under thermal nonequilibrium conditions a system of two phonons is used as in Eqs. (7) and (8). In this case, the "lattice temperature" is taken to be the acoustic phonon temperature (T_A), because this is the mode responsible for diffusion. Therefore, a comparison between the different cases is made through the lattice temperature of cases 1 and 2 and the acoustic temperature of case 3.

4. Results

To verify the simulation, output characteristics were plotted and compared with previously published results [15]. Due to insufficient information about the device manufacturing process, a few approximations were needed for features such as doping profiles. Also, device dimensions were modified slightly to attain symmetry (Fig. 2 and Table 1). Fig. 3 shows the comparative I_d–V_d plot for full SOI, partial SOI and bulk Si devices. For low gate voltages (4 and 8 V) the curves are similar to those reported by Perugupalli et al. [15]. Note that the three devices are expected to have similar I_d–V_d curves for the same gate voltage because the only difference between them is the buried oxide layer, which does not influence electrical performance appreciably at low gate voltage.

However, as gate voltage increases, nonequilibrium effects become prominent and cause the lattice temperature to rise. The buried oxide layer causes heat to be confined to the electrically active region. In Fig. 3 this effect is seen clearly for $V_g = 16$ V. The behavior of the three devices diverge after $V_d = 10$ V. The curve also undergoes transconductance compression at high gate and drain voltages, and therefore the drain current decreases with an increase in drain voltage. The drain current decreases primarily due to a reduction in mobility as carrier velocities saturate, which in turn is attributed to increased carrier-phonon scattering [10]. In the bulk device, the silicon region provides a conductive path for heat dissipation from the active region. The partial SOI device presents a higher resistance to heat flow due to the buried oxide layer. The full SOI device suffers from the highest heat confinement and thus exhibits the most divergent behavior. Note that silicon dioxide has a very low thermal conductivity (1.4 W/mK) compared to silicon (148 W/mK) and acts as a barrier to heat diffusion in the device.

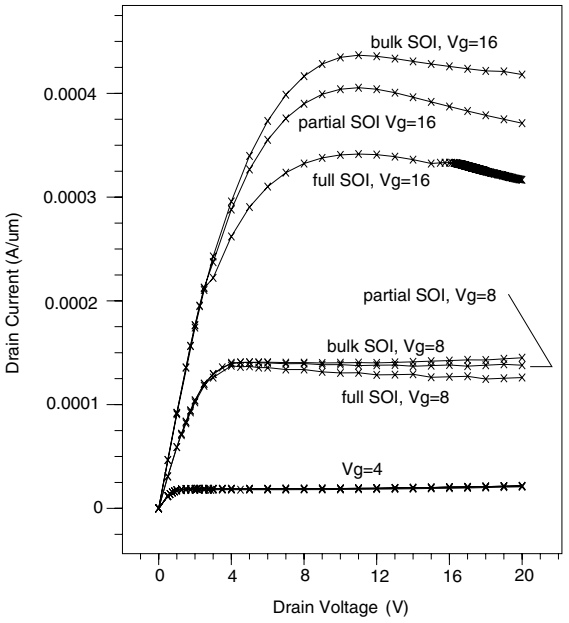

Fig. 3. I_d–V_d plot for the three devices at different V_g.

A significant observation is related to the regions associated with localized heating and to the development of hot spots with time. As described previously, three different models are considered for the energy transport. For the Joule heating model (Case 1), the localized heating is maximum under the gate on the drain side for the SOI device. The electric field and electron current density are both high in the LDD region (Eq. (9)), and the thermal source is largest in this region. With time, however, thermal diffusion occurs and the temperature profiles spread over the entire device. Fig. 4(a) and (b) show the thermally interesting region of the SOI device

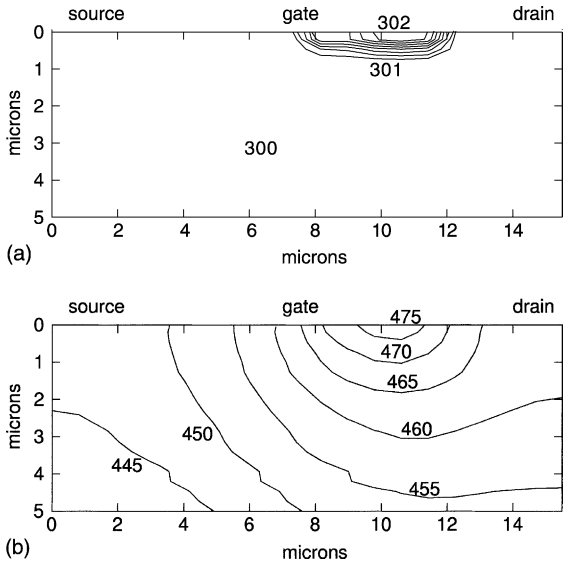

Fig. 4. Lattice temperature due to Joule heating: (a) $t = 1$ ns, (b) steady-state.

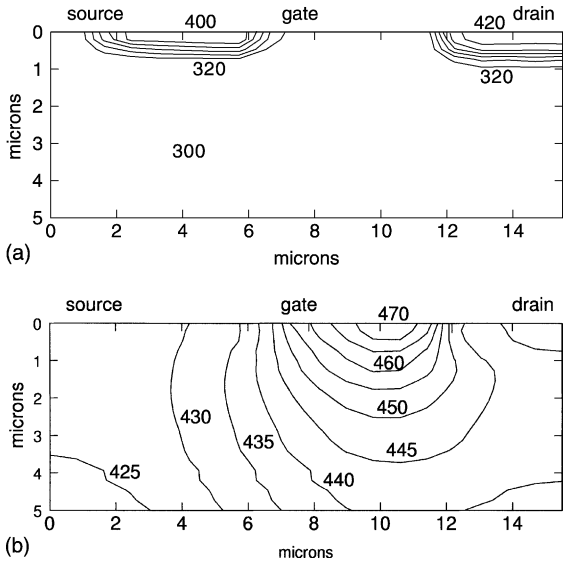

Fig. 5. Lattice temperature due to scattering: (a) $t = 1$ ns, (b) steady-state.

(above the buried oxide layer) for short times and steady-state respectively. Because of the insulating properties of the oxide layer, the largest gradient exists here and the localized heating is better demonstrated. Below the layer (not shown) the problem is reduced to one-dimensional conduction.

The two scattering models (Case 2 and Case 3), exhibit a different heating pattern than the Joule heating case. For the immediate discussion, the two scattering models are equivalent and no significant difference is noted. For both, two distinct hot spots are observed in the source and drain-doped regions at very short times ($t = 1$ ns) as shown in Fig. 5(a). This behavior can be explained by examining the energy transport mechanism between electrons and the lattice. Because transport relies on scattering of particles, the energy transfer occurs only where the electron density is large. This circumstance occurs on either side of the gate. On the source side, electrons are crowded by the depletion region, resulting in considerable electron density and increased collisions both between electrons and between electrons and phonons (or lattice). On the drain side, the doping provides collision sites for electrons and phonons. Under the gate where the Joule heating model predicted localized heating the electrons accelerate nearly ballistically meaning there is little energy transfer to the surrounding lattice.

The difference in the temperature distribution for short times is further verified by examining the mean free path (MFP), which is proportional to the electron velocity,

$$l_{\mathrm{MFP}} = v_{\mathrm{e}}\tau_m \tag{11}$$

where v_{e} is the electron velocity as calculated by ATLAS and the momentum scattering time constant is $\tau_m = 4.7$ ps. The estimate of the MFP is on the order of the device dimensions in the gate and LDD regions. In fact, the maximum mean free path is observed in the LDD region. Thus, the electrons undergo nearly ballistic transport in the LDD region. This result indicates that little energy would be transferred from electrons to the lattice by scattering in the LDD region. Electrons accelerated ballistically in the channel and LDD regions scatter in the drain region, losing their energy to the lattice.

At steady-state, the thermal energy has diffused to mitigate the distinction of the location of the two generation regions in Fig. 5(b). In fact, the diffusion of thermal energy nearly recovers the temperature distribution compared to the Joule heating case. However, because the source term is nonlinear, steeper gradients occur compared to the Joule heating case.

From the steady-state lattice temperature distributions alone, it appears that there is little difference between the scattering models. However, the extent of thermal nonequilibrium that is included in the model of Case 3 and not in the model of Case 2 can be estimated from the difference in the temperatures of the optical and acoustic phonons. Fig. 6 shows the time development of acoustic and optical phonon temperatures. It can be seen that at very short times, the energy transport from electrons to optical phonons dominates the problem resulting in nonequilibrium. Thus, the temperature of optical phonons increases more rapidly. As time increases, optical phonons transfer their energy to acoustic phonons. Thus, the temperature of acoustic phonons increases and eventually equilibrates with that of optical

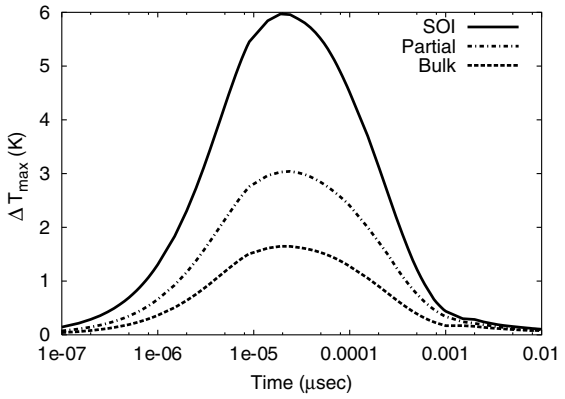

Fig. 6. Maximum temperature difference between phonon temperatures as a function of time. The difference gives an indication of the extent of thermal nonequilibrium in the system.

phonons at steady-state. This result is significant for devices with high switching speeds, such as in telecommunication circuits. The difference in the device configurations is also highlighted in Fig. 6, which shows that the SOI device experiences a higher degree of nonequilibrium than the other two devices. This figure also suggests that partial SOI, while providing good electrical isolation of the device, can lessen some of the effects of nonequilibrium seen by SOI devices.

The transport processes are governed largely by the scattering time constants. Because of the disparity of the order of magnitude of the different scattering rates, optical phonons are not able to transfer their energy to acoustic phonons as efficiently as the energy is transfered from electrons to optical phonons. The difference between optical and acoustic phonon temperatures, which is a measure of the extent of thermal nonequilibrium, is calculated for a full SOI device for a gate voltage of 16 V. The maximum temperature difference (6 K) is relatively small, suggesting that the level of nonequilibrium may be insignificant. However, the present simulations have no feedback mechanism to determine if the difference is physical or if electrical performance is affected. Note that the areas of high temperature difference, which occur under the source side of the gate and under the drain, are also the areas of high electric field in the device. In the presence of high electric fields, electrons are accelerated and become highly energetic. This energy is rapidly ($\tau \approx 100$ fs) and efficiently passed on to optical phonons. However, the interaction between optical and acoustic phonons is much slower in comparison ($\tau \approx 10$ ps). Thus, optical phonons are not able to transfer their energy to acoustic phonons fast enough, leading to thermal nonequilibrium. This confinement of thermal energy causes a higher rate of interaction with electrons, which in turn causes electron velocity saturation and reduction of drain current. Note that these effects are observable at very short time scales ($\tau \approx 1$ ps–1 ns).

5. Conclusions

A fundamental result of this work is that electrical characteristics of power devices are closely coupled with nonequilibrium thermal effects. In the analysis, the onset of thermal nonequilibrium was observed. The findings lead us to believe that devices with similar or smaller dimensions with short time scale features are susceptible to thermal nonequilibrium effects.

Emphasis was placed on three different thermal models to evaluate the extent and locations of thermal nonequilibrium. The difference between the scattering models and Joule heating model were significant for short time scales. At steady-state, the difference between the scattering model and the Joule heating was apparent but probably not significant. Further investigation using a fully coupled computational method is planned to determine the effect of each model on electrical performance. The difference between the two scattering models (electron–lattice scattering and the phonon model) were minor. However, the present device is relatively large compared to modern power devices and nonequilibrium effects become more pronounced as length scales shrink. Therefore, because nonequilibrium was observed at these large scales, smaller devices deserve additional investigation to determine the extent of nonequilibrium.

Additional emphasis was placed on comparing bulk Si, partial SOI and full SOI devices to study the extent of nonequilibrium in each. In the electrical simulations, output characteristics of full SOI devices differed considerably from the equilibrium condition (Joule heating model). The variation is attributed to the thermal trapping effects of the buried oxide layer. Output characteristics of the partial SOI device were found to vary to a lesser extent. The bulk Si device exhibits behavior closest to an equilibrium condition. The fact that nonequilibrium was observed in the SOI case compared to the bulk case further reinforces the possibility of significant nonequilibrium behavior in smaller devices. Analysis of acoustic and optical phonons has assisted in identifying time scales for which thermal nonequilibrium could be significant; thermal nonequilibrium does not play a significant role in steady-state calculations. However, potentially strong nonequilibrium effects may occur for high-speed transient conditions with temporal features less than nanoseconds.

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