

NON-EQUILIBRIUM THERMAL EFFECTS IN POWER TRANSISTORS

Ashok Raman, D.G.Walker and T.S.Fisher*

Department of Mechanical Engineering
Vanderbilt University
Nashville, TN 37235

ABSTRACT

This work addresses electro-thermal simulation of LDMOS devices and associated non-equilibrium effects. Simulations have been performed on three kinds of LDMOS i.e. bulk Si, partial SOI and SOI, with a view to compare the extent of non-equilibrium in each. Phonon temperature contours and electron energies were analyzed in each case. The results indicate that, under similar operating conditions, non-equilibrium is most pronounced in case of SOI devices. A comparison between transient and steady state acoustic phonon temperatures indicates that the mechanisms and device regions associated with non-equilibrium could be very different depending on the switching rate. Analysis of the effective mean free path of carriers in the active region shows that the primary source of heat generation is carrier-phonon scattering and not Joule heating as is generally assumed. Under steady state conditions however, device heating due to these two mechanisms looks very similar.

NOMENCLATURE

C bulk thermal capacitance of Si
 C_a acoustic phonon thermal capacitance
 C_o optical phonon thermal capacitance
 D thermal diffusivity
 G generation rate of holes or electrons
 H generation term in bulk conduction equation
 J current density
 k bulk thermal conductivity of Si
 k_a thermal conductivity of acoustic phonons
 k_b Boltzmann constant
 L_g gate length
 m effective mass
 N_D doping concentration
 q electron charge
 T_a acoustic phonon temperature
 T_o optical phonon temperature
 T_L lattice temperature
 S energy flux
 V voltage
 v carrier velocity
 W energy density loss rate
 ϵ local permittivity
 μ mobility
 η carrier density
 κ electron thermal conductivity
 ψ electrostatic potential

ρ local space charge density

τ_{e-L} electron-lattice scattering time constant

INTRODUCTION

MOSFETs are widely used in a variety of power systems because of certain inherent characteristics. In high speed switching applications these devices offer low on-state resistance [1]. In high frequency RF applications they exhibit low capacitance and high gain (LDMOS) or high stability (VDMOS) [2]. MOS can also be integrated with signal processing circuits to form 'smart chips' and IPLSIs [3]. The present work focuses on LDMOS, which is better suited for high frequency applications such as telecommunication circuits. These lateral surface effect devices are however, susceptible to hot carrier currents that induce several breakdown mechanisms. Various efforts have been directed towards characterizing hot carrier effects in LDMOS, and suggestions have been made to mitigate such effects [4]-[6]. These attempts represent a modest improvement in thermal management, and the devices are still likely to exhibit thermal problems. It is for this reason that thermal simulations of LDMOS are crucial for accurate estimates of device performance.

Numerical simulations are widely used to understand device physics and predict non-equilibrium behavior in sub-micron devices, because the length and time scales involved are not easily amenable to experimental analysis. It is thus imperative that the simulation models used be as accurate as possible. Apanovich et al. [7] report that the coupling between non-local charge transport and non-isothermal effects are significant in SOI devices on account of the low thermal conductivity of the buried oxide and the parasitic bipolar effect. Non-isothermal models were found to predict impact ionization and secondary breakdown more accurately than isothermal models, thus highlighting the influence of lattice heating on the electrical behavior of devices. Wachutka [8] describes the source of non-isothermal effects in electronic devices in great detail. The Wachutka model for device thermal characterization accounts for non-equilibrium phenomena such as generation-recombination, Joule and Thomson heating. The model is also valid for transient simulations where the difference in thermal behavior of the two modes of lattice vibrations, the optical and acoustic phonons, is most pronounced. It is this difference between phonons that is responsible for thermal non-equilibrium in the active region of the device.

Lai and Majumdar [9] have developed a coupled electro-thermal model for studying non-equilibrium in sub-micron

*Address all correspondence to this author
e-mail : tim.fisher@vanderbilt.edu

silicon MOSFETs. They have determined the highest electron and lattice temperatures to be under the drain side of the gate electrode, which also corresponds to the region of highest electric field, and in turn the region where non-equilibrium effects such as impact ionization and velocity overshoot are maximum. Majumdar et al [10] have analyzed the variation of hot electron and associated hot phonon effects in GaAs MESFETs. These hot carrier effects were observed to decrease the output drain current by as much as 15%. Thus, they conclude that both electron and lattice heating must be included in the analysis of electrical behavior of a device.

An important structural modification that has been suggested to overcome some of the inherent deficiencies of bulk Si LDMOS and SOI, is the partial SOI device. Bulk Si LDMOS, though they possess excellent thermal conduction properties, often suffer from large leakage currents. SOI devices were developed to isolate electrical activity. The buried oxide layer in these devices acts as an electrical insulator that minimizes leakage currents. However the oxide layer also acts as a barrier to thermal dissipation. This spatial confinement of local heating adversely affects the electrical performance of the device, as demonstrated by the literature cited above. In contrast to SOI, the buried oxide layer in partial SOI does not extend across the entire length of the device. Instead, a ‘silicon window’ under the drain region provides an efficient path for heat to diffuse away from the electrically active region. Figure 1 shows cross-sectional views of these LDMOS devices.

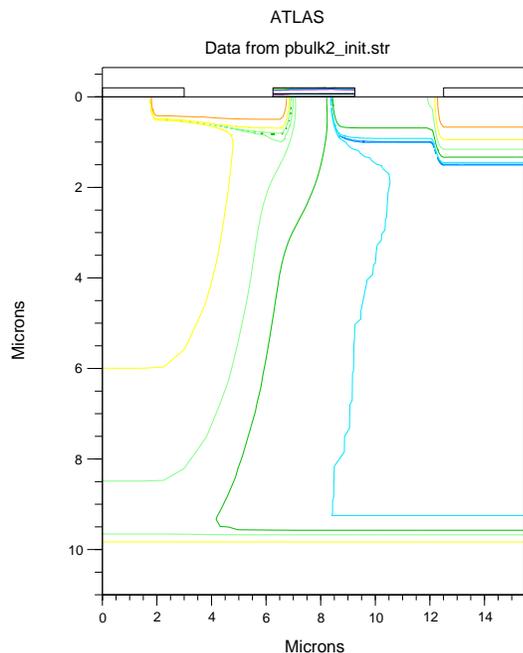


Figure 1 (a): Cross-sectional view of the bulk Si device used in this work. The partial SOI had a buried oxide layer that extended to a length of 12.5 μm as shown in Fig 1(b) while in the SOI case the oxide extended throughout the length of the device.

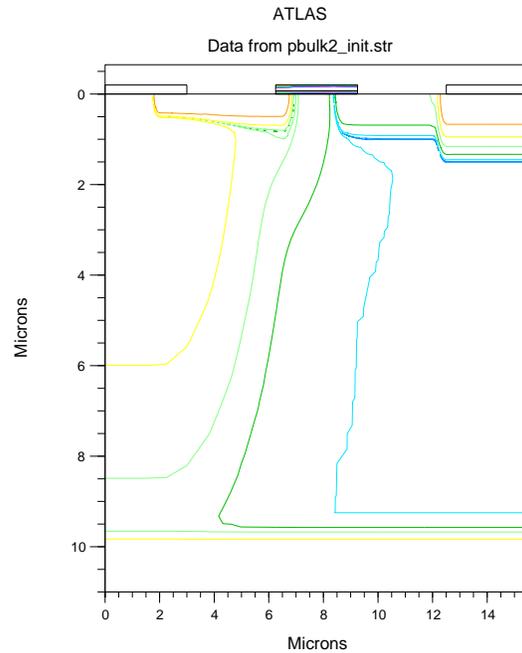


Figure 1 (b): Device technological parameters

This work compares the behavior of the three kinds of LDMOS, i.e. bulk Si, SOI and partial SOI, to determine the extent of non-equilibrium in each case. The SOI and partial SOI devices were analyzed with a primary aim of studying the influence of an insulator (oxide) layer within the device. Extensive DC simulations were performed to study the static behavior of the devices. Their thermal characteristics were compared to obtain qualitative information about non-equilibrium effects. The simulations were performed in an ‘uncoupled’ manner. The electrical characteristics were analyzed using a commercial package (ATLAS [11]), while the thermal behavior was studied using a custom-designed phonon solver. The I_d - V_d and temperature comparison plots for the three devices and the conclusions drawn from them are presented.

Lim et al [12] have earlier reported a comparison between self-heating effects in thin SOI and partial SOI devices, under both steady state and transient conditions. The present work deals with thick SOI and concentrates more on transient conditions, since non-equilibrium conditions are more likely to be observed under such conditions. However, the evolution into steady state is also considered for the sake of completeness. Emphasis has been laid on determining the actual source of lattice heating between scattering and Joule heating, as this is found to vary with time.

DEVICE STRUCTURE

The device structure and behavior was modeled after that of Perugupalli et al. [13], but incorporated certain modifications in doping profiles and thickness of the buried oxide layer. The threshold voltage was designed to be $V_t \sim 2.5\text{V}$ [Fig.2]. The SOI and partial SOI devices were modeled from the bulk device and had comparable

threshold voltages. The physical dimensions of the devices are listed in Table 1.

TABLE – 1 :
DEVICE DIMENSIONS

Parameter	Value (μm)
l_s	3.0
l_{so}	3.25
l_g	3.0
l_{idd}	3.0
l_d	3.0
t_{ox}	0.065
t_{epi}	9.0
t_{base}	4.0
t_{sub}	1.0

Gaussian doping profiles were used in this simulation with appropriate x- and y-direction roll-off distances. The source and drain regions were doped with $10^{20}/\text{cm}^3$ of phosphorus while the LDD region was doped with $10^{17}/\text{cm}^3$ of phosphorus. The substrate region in each device was doped with $10^{15}/\text{cm}^3$ of boron. In the bulk device, the p^+ sinker and p body were doped with $10^{19}/\text{cm}^3$ and $1.5 \times 10^{17}/\text{cm}^3$ boron respectively (Fig.1a). The source and drain contacts of the device were aluminum and were considered to be Ohmic contacts. For the sake of simplicity, the gate was also aluminum and the corresponding work function was used to solve for the threshold voltage. The finite element computational mesh comprised of 5194 nodes and 10000 triangles. A minimum spacing of 0.02 microns was specified. The maximum height and width were 0.5 microns each in the device substrate and epitaxial regions. The region immediately beneath the gate oxide had a very fine mesh in order to capture the gradients associated with the inversion layer. The region under the LDD and drain also had a fine mesh because large gradients were located in these regions. In such regions care must be taken to keep the minimum mesh spacing below the Debye length of the active region, in order to minimize errors created due to discretization [9].

SIMULATIONS

In this work, the electrical and thermal characteristics of the devices were analyzed in an ‘uncoupled’ manner. The commercial simulator (ATLAS) was used to perform the electrical characterization. Results from the electrical analysis, such as electron concentrations, electric fields and electron velocity, were imported into a custom-designed phonon solver. The results of this phonon solver are not coupled back to the electrical analysis. The results generated are thus, only qualitative, but still provide valuable insight into the interaction between the electronic and phonon systems. Efforts are underway to couple the electrical and thermal solvers in order to get more accurate results.

Electrical Simulations-

DC simulations were performed to obtain I_d - V_d characteristics of the devices. The electrical characteristics were found using the energy balance model in ATLAS with

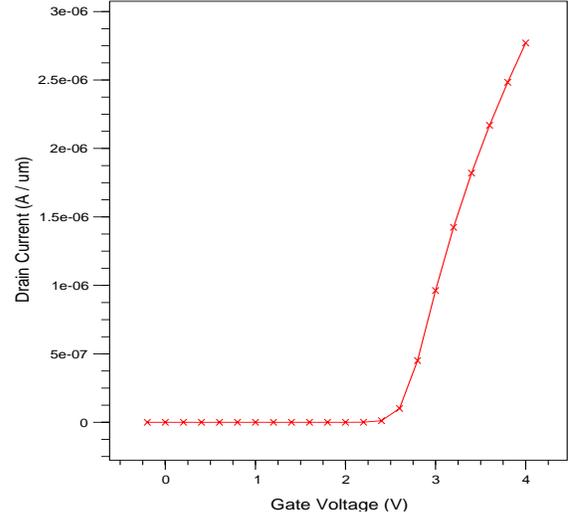


Figure 2: Threshold voltage for the bulk Si device. The partial SOI and SOI devices had similar behavior.

the lattice heat diffusion equation. The gate voltages were chosen to be 4, 8 and 16 V in each case. At each gate voltage the drain voltage was stepped up from 1 to 20 V in increments of 1 V. Comparative electrical studies were performed on the devices under similar operating conditions i.e. at a drain voltage of 20 V for each gate voltage. Note that all simulations were performed at steady state.

The energy balance model used in this study is essentially the hydrodynamic model along with the lattice heating equation. It incorporates effects such as diffusion associated with carrier temperatures and dependence of impact ionization rates on carrier energy distributions [11]. This model consists of Poisson’s equation for determining the electric field distribution and the carrier continuity equation for determining the carrier concentration. These equations are solved in the Si region only. The equations used for energy flux and current density are given below:

$$\nabla \bar{S} = -\bar{J} \nabla \psi - W - \frac{3k_b}{2} \frac{\partial}{\partial t} (\eta T_n^*) \quad (1)$$

$$\bar{J} = qD \nabla \eta - \mu \eta \nabla \psi + q \eta D_n^T \nabla T_n \quad (2)$$

$$\bar{S} = -\kappa \nabla T_n - \left(\frac{k_b}{q} \right) \bar{J} T \quad (3)$$

Accurate MOSFET simulations call for the use of inversion layer specific mobility models. This is due to the high scattering that occurs near the channel-gate oxide interface. In this simulation a comprehensive model that takes into account the effect of transverse electric field, doping profile and carrier temperature distribution, was employed. It also

includes the dependence of mobility on the parallel electric field, which is important near carrier saturation velocities.

The lattice heat diffusion equation given as

$$C \frac{\partial T_L}{\partial t} = \nabla \cdot (k \nabla T_L) + H \quad (4)$$

was included to determine the extent of energy transfer between the carrier and the lattice, and to study the variation of lattice temperatures with input bias. Here H is the heat source and is modeled after the rigorous physical model proposed by Wachutka [8]. It includes micro-scale effects such as generation-recombination and impact ionization, and bulk effects like Joule heating and Peltier and Thomson effects. A constant temperature sink (300 °K) was used as the thermal boundary at the bottom of the device (Dirichlet). All other boundaries were considered to be insulated (Neumann). Non-local transport effects in the device were modeled by including Selberherr's model [14] for impact ionization and the Shockley-Read-Hall model for carrier recombination.

The temperatures considered here are the local lattice temperatures. ATLAS has certain built-in relations for determining properties based on local lattice temperatures [8]. The temperature dependent lifetime of the carriers in the recombination model was assumed to be the default value of 10^{-7} seconds.

Note that an exact determination of the electron and phonon energies in the non-equilibrium regime would involve solving the Boltzmann Transport Equation (given below) for each of them:

$$\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla f + \vec{F} \cdot \frac{\partial f}{\partial \vec{p}} = \left(\frac{\partial f}{\partial t} \right)_{scat} \quad (5)$$

where f represents the distribution of particles, p represents the momentum vector and F is the force applied on the system by the electric field. The right side represents the rate of change of particle distribution due to scattering. Solving the transport equation requires a lot of computational effort and an easier approach is to use the hydrodynamic equations of electron and phonon transport [9]. The hydrodynamic equations are derived from the Boltzmann transport equation by employing the relaxation time approximation and taking appropriate moments for momentum and energy. The scattering term under these approximations can be represented by

$$\left(\frac{\partial f}{\partial t} \right)_{scat} = \frac{3\rho k_B}{2} \left(\frac{T_e - T_L}{\tau_{e-L}} \right) \quad (6)$$

This term represents energy transfer from electrons to the lattice and is a source of heat for the lattice. As the

magnitude of this term increases, the device is pushed further away from equilibrium.

Thermal Simulations–

Thermal analysis of the devices consisted of solving the energy equations for optical and acoustic phonons. These equations are given as [15]

$$C_{LO} \frac{\partial T_{LO}}{\partial t} = \frac{3\rho k_B}{2} \left(\frac{T_e - T_{LO}}{\tau_{e-LO}} \right) + \frac{\rho m^* v^2}{2\tau_{e-LO}} - C_{LO} \left(\frac{T_{LO} - T_A}{\tau_{LO-A}} \right) \quad (7)$$

$$C_A \frac{\partial T_A}{\partial t} = \nabla \cdot (k_A \nabla T_A) + C_{LO} \left(\frac{T_{LO} - T_A}{\tau_{LO-A}} \right) + \frac{3\rho k_B}{2} \left(\frac{T_e - T_A}{\tau_{e-A}} \right) \quad (8)$$

2 phonon energy equations from Majumdar

Equation 7 describes energy conservation for optical phonons. C_{LO} represents the heat capacity of optical phonons. The first two terms on the right side represent energy inputs from electrons, while the third term is the energy loss to acoustic phonons. Equation 8 describes energy conservation for acoustic phonons. The terms are quite similar to those in Eq 7, with one important difference. Acoustic phonons possess finite group velocity and participate in heat diffusion. Optical phonons however, have negligible group velocity and cannot diffuse heat. They provide an efficient intermediary system for heat transfer from the source (electrons) to the sink (acoustic phonons).

The thermal analysis software was developed from a commercial, object-oriented mathematical solver package called Diffpack [16]. The underlying idea was to solve the two energy equations above, but with an interface with ATLAS, in order to read in results of the electrical simulation. The analysis was performed for very short time steps (\sim 1ps-1ns) to study the transient behavior of phonons. The time-development of the temperature profiles of the two phonons to attain steady state, was also studied. It should be mentioned at this point that results of the electrical simulation contained steady state values, and their use for generating transient phonon results yielded qualitative results.

The numerical solution technique employed was SSOR, with a relaxation parameter of #####. The energy equations were discretized by means of an in-built FEM algorithm in Diffpack. The thermal boundary conditions applied are shown below

$$T = 300 \text{ K, on the bottom of the device}$$

$$\text{Thermal insulation, at the other 3 boundaries}$$

Since the device is analyzed using two different software packages, an energy balance is performed between the ATLAS and Diffpack simulations. This ensures that in both

the cases, the overall thermal energy is the same, and that different thermal distributions are created only due to the difference in device phenomena. Ideally, the electron and phonon systems should be solved in a coupled manner. The results obtained by this uncoupled simulation, however, provide insight into the mechanisms and regions associated with electron-phonon energy exchange, and the resulting non-equilibrium effects.

Results on phonon analysis are presented and discussed in the next section.

RESULTS

To verify the simulation, output characteristics were plotted and compared with previously published results [13]. Due to insufficient information about the device manufacturing process, a few approximations had to be made for features such as doping profiles. Also, device dimensions were modified slightly to attain symmetry (Fig 1 and Table I). Thus, the results are only expected to be qualitatively similar. Figure 3 shows the comparative I_d - V_d plot for SOI, partial SOI and bulk Si devices. For low gate voltages (4 V and 8 V) the curves are similar to those reported by Perugupalli et. al. [13]. Note that the three devices are expected to have similar I_d - V_d curves for the same gate voltage. This is because the only difference between them is the buried oxide layer, which does not influence electrical performance appreciably at low gate voltage. However as we increase the gate voltage, non-equilibrium effects become prominent and cause the lattice temperature to rise. The buried oxide layer causes this heat to be confined to the electrically active region. In Fig 3 this effect is seen clearly for $V_g=16$ V. The behavior of the three devices diverge after $V_d=10$ V. The curve also undergoes transconductance compression at high gate and drain voltages, and therefore the drain current decreases with an increase in drain voltage. This is primarily due to a decrease in mobility as carrier velocities saturate, which in turn is attributed to increased carrier-phonon scattering [9]. The bulk device has the best heat conduction capability. In other words, energy transfer from the electronic system to phonons is very efficient in the absence of the buried oxide layer, and consequently there is no thermal build-up. The partial SOI device exhibits more energy trapped in the active region than the bulk device but the silicon window permits this heat to partially dissipate into the substrate region. The SOI device suffers from the highest heat confinement and thus exhibits the most divergent behavior. Note that silicon oxide (3 W/mK) has a very low thermal conductivity compared to silicon (148 W/mK), and as Eq 8 suggests, it acts as a barrier in heat diffusion in the device.

Analysis of the results of the thermal simulations provided insight into the influence of lattice heating (acoustic phonons) on electron behavior. Figure 4 shows the time-development of acoustic and optical phonon temperatures. It can be seen that at very low time steps, electronic energy is transferred more efficiently to optical phonons. Thus, the temperature of optical phonons increases more rapidly. As time increases, optical phonons transfer their energy to acoustic phonons, which actually participate in heat diffusion. Thus, the temperature of acoustic phonons

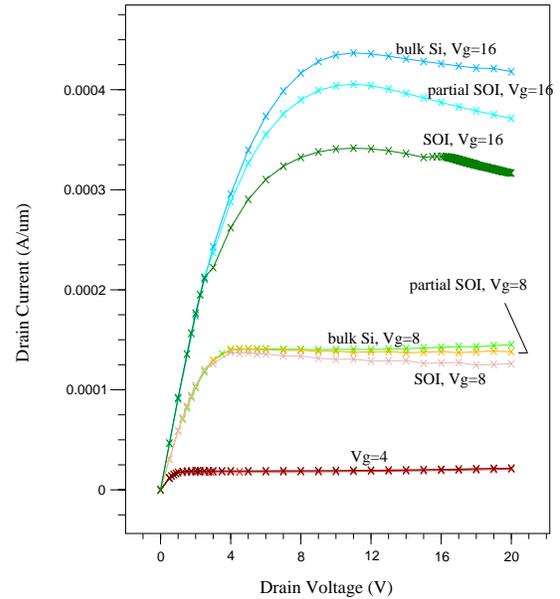


Figure 3 : I_d - V_d plot for the three devices at different V_{gs} .

increases and finally catches up with that of optical phonons at steady state. This result is very significant for devices which have high switching speeds, such as switches in telecommunication circuits. At very short time intervals, optical phonons are not able to transfer their energy to acoustic phonons. This results in thermal energy getting trapped in the active region of the device [15]. This effect is more significant for SOI devices where the buried oxide layer provides an added barrier to heat conduction.

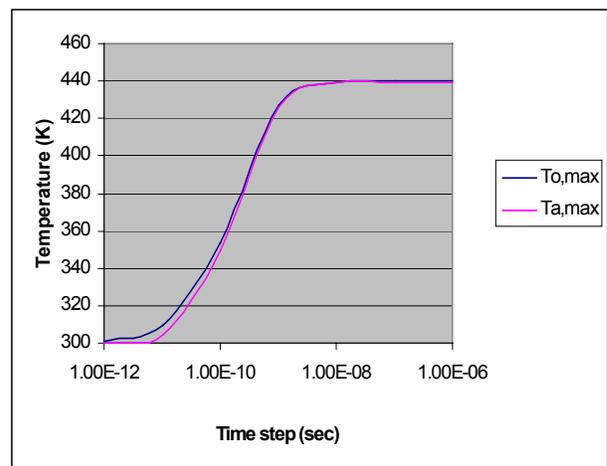


Figure 4: Time development of APE-OPE temperatures

Since thermal non-equilibrium is caused by the energy difference between optical and acoustic phonons, some

interesting results were drawn from the plots of optical and acoustic temperatures inside the device. The region of maximum optical phonon temperature need not be the region of maximum acoustic phonon temperature. This is attributed to the negligible group velocity of optical phonons, as proposed by Lai and Majumdar [9]. The difference between optical and acoustic phonon temperatures is calculated and plotted throughout an SOI device for a gate voltage of 16V (Fig 5). It is observed that the maximum temperature difference occurs near the drain end of the gate electrode. This is also the region of maximum electric field in the device. In the presence of high electric fields, electrons are accelerated and they become very energetic. This energy is rapidly ($\tau \sim 100$ fs) and efficiently passed on to optical phonons. However, the interaction between optical and acoustic phonons is much slower in comparison ($\tau \sim 10$ ps). Thus, optical phonons are not able to transfer their energy to acoustic phonons fast enough, leading to thermal build-up. This confinement of thermal energy causes a higher rate of interaction with electrons, which in turn causes electron velocity saturation and reduction of drain current. Note that these effects are significant at very short time scales ($\tau \sim 1$ ps – 1ns).

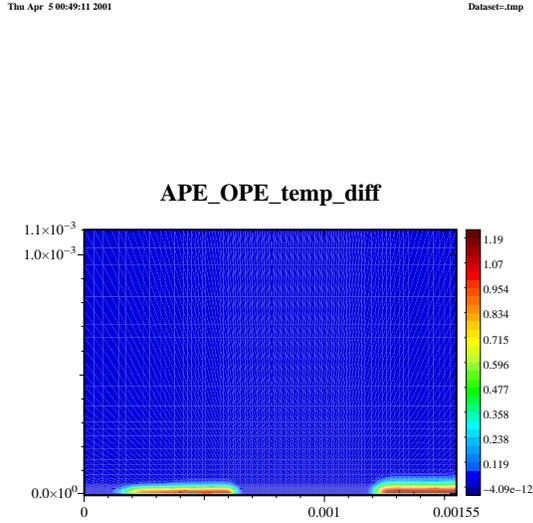


Figure 5: Temperature difference plot between APE and OPE for SOI LDMOS at $V_g=16V$

Another significant observation concerned the physical source of internal device heating. It is assumed that the macroscopic phenomena of Joule heating can be used to predict device self-heating. However, analysis of acoustic phonon temperatures at different time intervals revealed

that the mechanism responsible for device heating is electron-phonon scattering. As eq –8 illustrates, the energy associated with electron-phonon scattering depends on the temperature difference between the two systems and the carrier concentration. In an NMOS, as is used in this work, maximum carrier concentration is found in the source, LDD and drain regions. At time steps on the order of 1 ps, it is observed that maximum acoustic phonon temperatures are indeed found in the source and drain regions. As the time interval increases, these source terms increase until they reach a maximum value ($\tau \sim 1\mu s$). Beyond this, the source term remains constant, although thermal diffusion occurs from these two hot spots. In course of diffusion, the hot spot on the source side of the device slowly engulfs the hot spot on the drain (Figure 6). The resultant hot spot ($\tau \sim 1ms$) is seen on the drain side under the gate electrode. Thus, at steady state the heat source due to scattering looks very similar to the heat source due to Joule heating. However, as the time scales decrease (as in the case of high speed switches), the Joule heating model would not be accurate any longer. The scattering source term would have to be used for accurate device simulation.

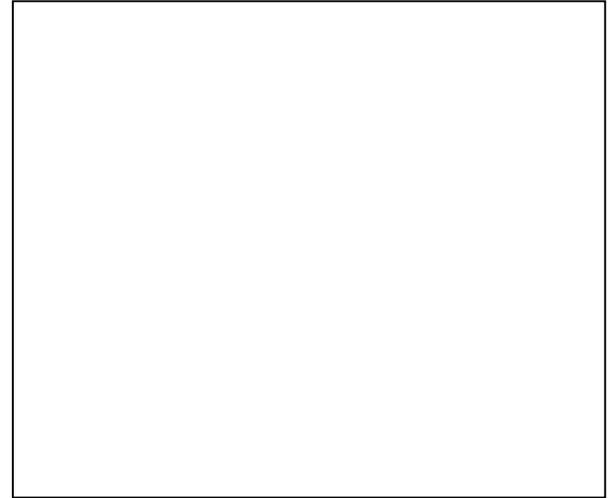


Figure 6: Acoustic and optical phonon temperature plots for different time intervals

Mean free path values for the carriers were calculated by the following formula

$$l = v_e * \tau \quad (9)$$

where v_e is the electron velocity as calculated by ATLAS. Note that the variation of electron velocity with doping profiles and transverse and longitudinal electric fields, is accounted for in the electron mobility. τ is the time constant associated with electron scattering and is assumed to be constant (following the practice of ATLAS). A plot (Fig 7) of the carrier mean free paths as determined by eq 9, indicates that the maximum mean free path is observed in the LDD region. Thus, the electrons undergo near ballistic transport in the LDD region. This indicates that not

much energy would be transferred from electrons to the lattice in the LDD region, as is predicted by the Joule heating model. This further strengthens the argument that electron scattering is the physical model for determining the source of device self-heating.

CONCLUSIONS

A fundamental result of this work is that electrical characteristics of power devices are intimately coupled with non-equilibrium thermal effects. Emphasis was laid on comparing bulk Si, partial SOI and SOI devices, to study the extent of non-equilibrium in each. In the electrical simulations, it was observed that the output characteristics of SOI devices differed considerably from the equilibrium condition (drift-diffusion model). This is attributed to the thermal trapping effects of the buried oxide layer. Output characteristics of the partial SOI device were found to vary to a lesser extent. The bulk Si device exhibits behavior closest to the equilibrium condition. Thus, non-equilibrium effects are most pronounced in SOI devices.

Analysis of acoustic and optical phonons revealed that the mechanism and device region associated with self-heating could differ depending on the time scale of interest. Also, the physical source of thermal energy is identified to be micro-scale scattering between electrons and phonons, and not the macro-scale Joule heating phenomenon as is generally believed. Analysis of carrier mean free paths further embellishes this fact.

Future work would be directed towards coupling the electron and phonon systems, in order to get more accurate estimates of device non-equilibrium. The influence of doping profiles and device dimensions on non-equilibrium effects would also provide insight into scaling phenomena.

ACKNOWLEDGMENTS

The authors would like to acknowledge Dr. Ron Schrimpf, Claude R.Cirba and Jeremy Ralston-Good in the Dept. of Electrical Engg. And Computer Science at Vanderbilt University for their help with the simulation processes, and in understanding device physics. This work was made possible by a Vanderbilt University Discovery Grant and an NSF Career Award (CTS-9983961).

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